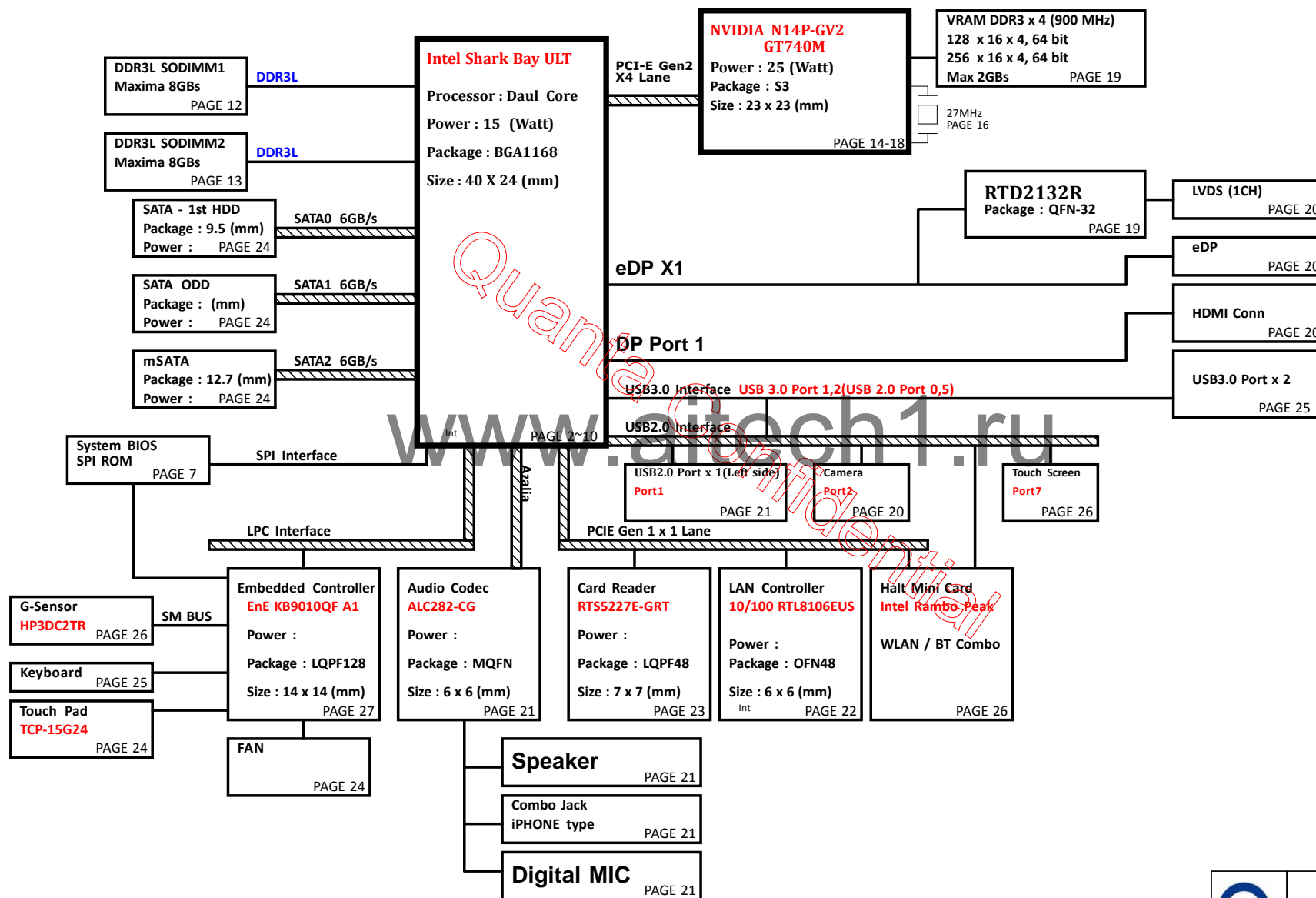


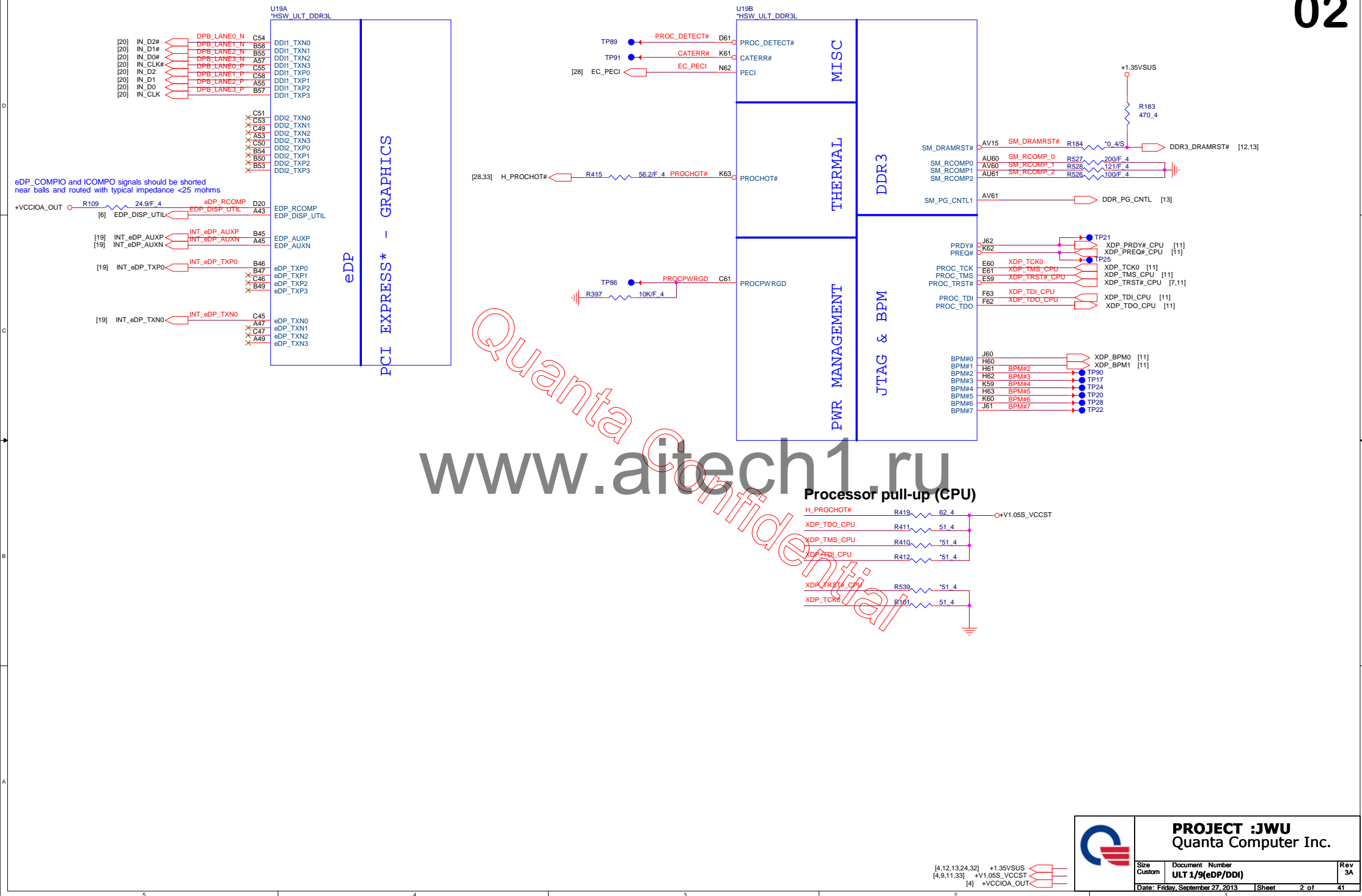
JWU DIS(14")

Intel Shark Bay ULT Platform Block Diagram

PCB 6L STACK UP

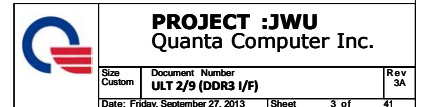
LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(Low)
 LAYER 5 : SVCC
 LAYER 6 : BOT

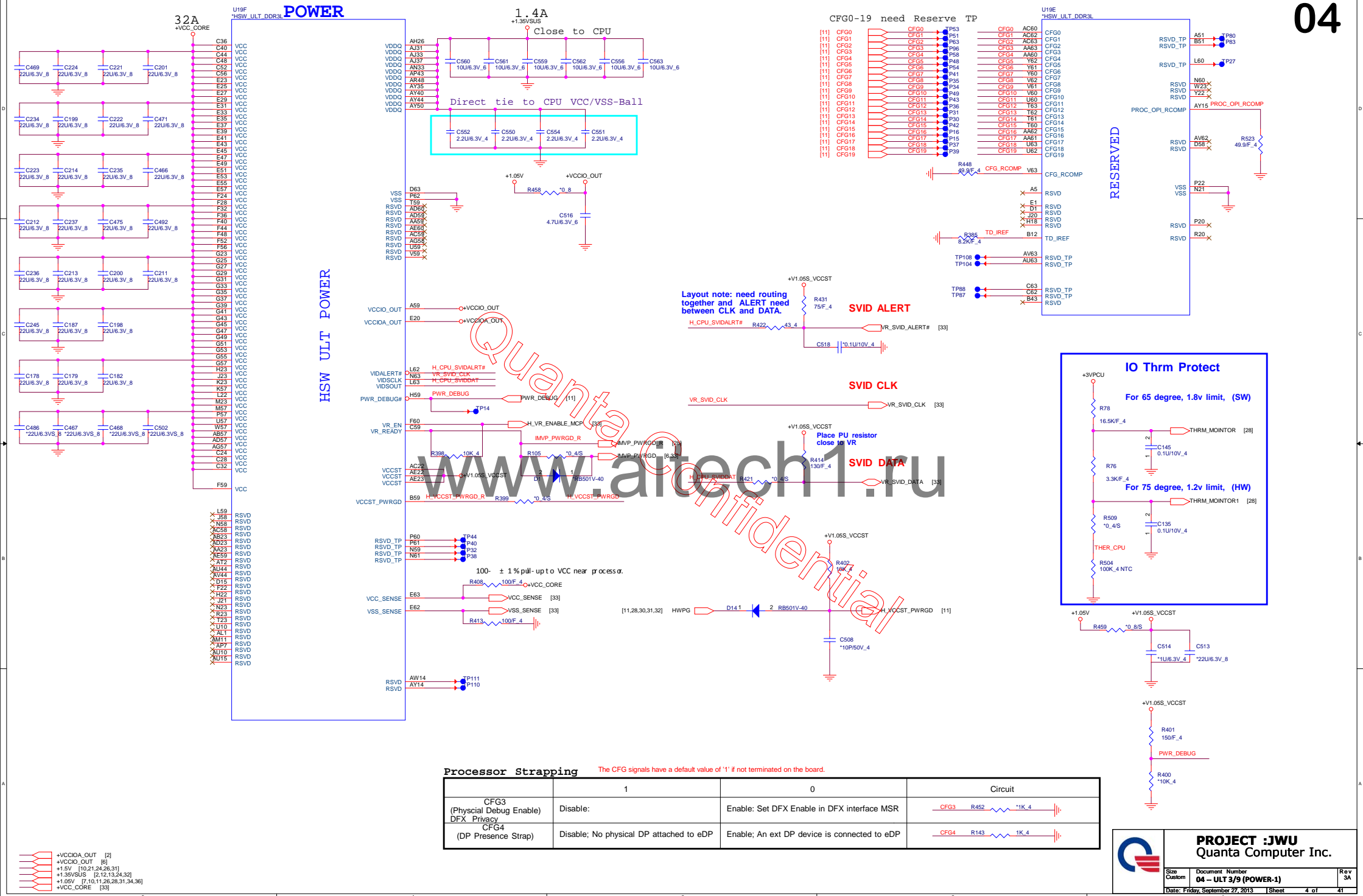


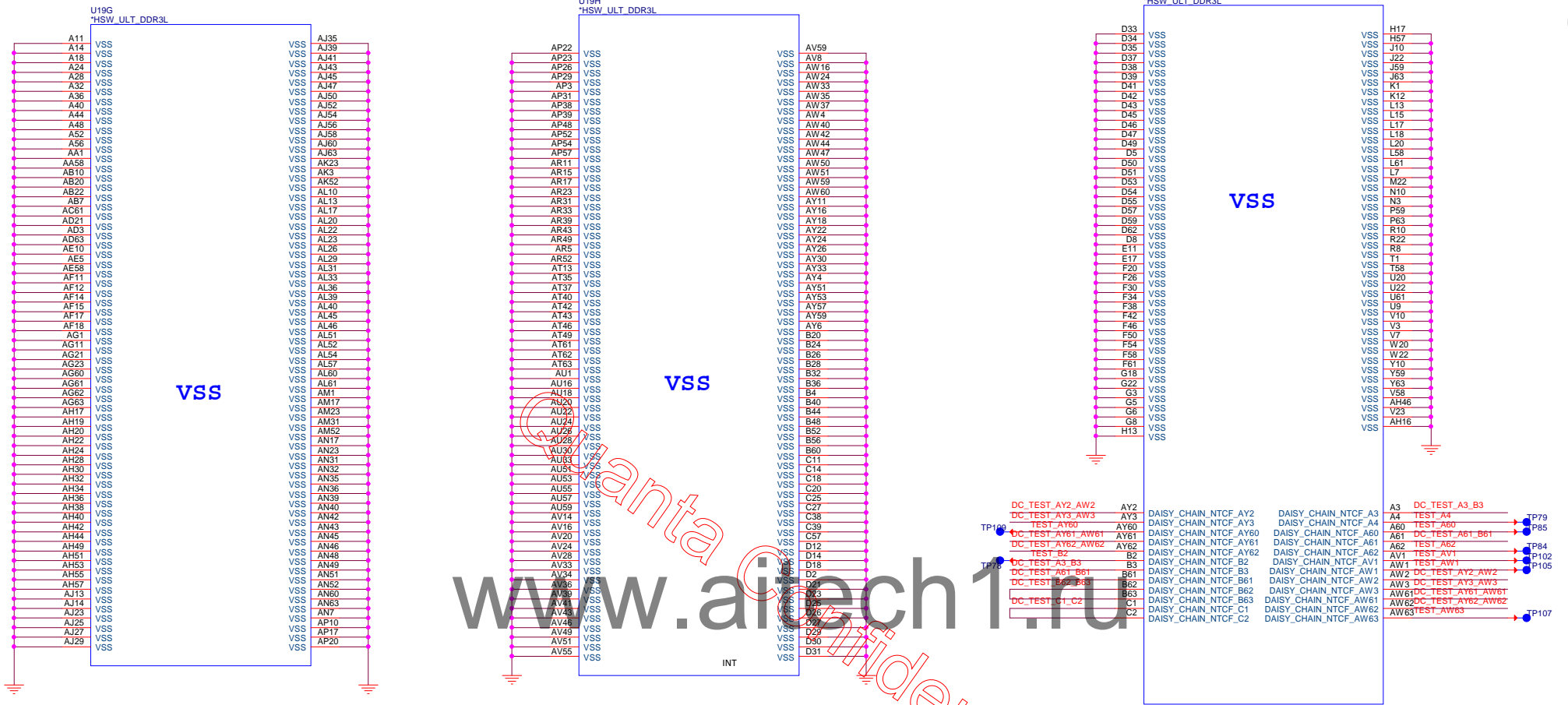


Top Section: Buses and Memory

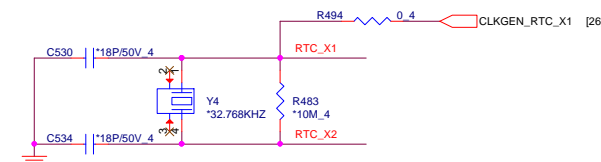
Component	Address Range
M. A, CS#0	[12]
M. A, CS#1	[12]
M. B, DQ#0	AK26
M. B, DQ#1	AK26
M. B, DQ#2	AK25
M. B, DQ#3	AK25
M. B, DQ#4	AK25
M. B, DQ#5	AK25
M. B, DQ#6	AK25
M. B, DQ#7	AK25
M. B, DQ#8	AK25
M. B, DQ#9	AK25
M. B, DQ#10	AK25
M. B, DQ#11	AK25
M. B, DQ#12	AK25
M. B, DQ#13	AK25
M. B, DQ#14	AK25
M. B, DQ#15	AK25
M. B, DQ#16	AK25
M. B, DQ#17	AK25
M. B, DQ#18	AK25
M. B, DQ#19	AK25
M. B, DQ#20	AK25
M. B, DQ#21	AK25
M. B, DQ#22	AK25
M. B, DQ#23	AK25
M. B, DQ#24	AK25
M. B, DQ#25	AK25
M. B, DQ#26	AK25
M. B, DQ#27	AK25
M. B, DQ#28	AK25
M. B, DQ#29	AK25
M. B, DQ#30	AK25
M. B, DQ#31	AK25
M. B, DQ#32	AK25
M. B, DQ#33	AK25
M. B, DQ#34	AK25
M. B, DQ#35	AK25
M. B, DQ#36	AK25
M. B, DQ#37	AK25
M. B, DQ#38	AK25
M. B, DQ#39	AK25
M. B, DQ#40	AK25
M. B, DQ#41	AK25
M. B, DQ#42	AK25
M. B, DQ#43	AK25
M. B, DQ#44	AK25
M. B, DQ#45	AK25
M. B, DQ#46	AK25
M. B, DQ#47	AK25
M. B, DQ#48	AK25
M. B, DQ#49	AK25
M. B, DQ#50	AK25
M. B, DQ#51	AK25
M. B, DQ#52	AK25
M. B, DQ#53	AK25
M. B, DQ#54	AK25
M. B, DQ#55	AK25
M. B, DQ#56	AK25
M. B, DQ#57	AK25
M. B, DQ#58	AK25
M. B, DQ#59	AK25
M. B, DQ#60	AK25
M. B, DQ#61	AK25
M. B, DQ#62	AK25
M. B, DQ#63	AK25
M. B, DQ#64	AK25
M. B, DQ#65	AK25
M. B, DQ#66	AK25
M. B, DQ#67	AK25
M. B, DQ#68	AK25
M. B, DQ#69	AK25
M. B, DQ#70	AK25
M. B, DQ#71	AK25
M. B, DQ#72	AK25
M. B, DQ#73	AK25
M. B, DQ#74	AK25
M. B, DQ#75	AK25
M. B, DQ#76	AK25
M. B, DQ#77	AK25
M. B, DQ#78	AK25
M. B, DQ#79	AK25
M. B, DQ#80	AK25
M. B, DQ#81	AK25
M. B, DQ#82	AK25
M. B, DQ#83	AK25
M. B, DQ#84	AK25
M. B, DQ#85	AK25
M. B, DQ#86	AK25
M. B, DQ#87	AK25
M. B, DQ#88	AK25
M. B, DQ#89	AK25
M. B, DQ#90	AK25
M. B, DQ#91	AK25
M. B, DQ#92	AK25
M. B, DQ#93	AK25
M. B, DQ#94	AK25
M. B, DQ#95	AK25
M. B, DQ#96	AK25
M. B, DQ#97	AK25
M. B, DQ#98	AK25
M. B, DQ#99	AK25
M. B, DQ#100	AK25
M. B, DQ#101	AK25
M. B, DQ#102	AK25
M. B, DQ#103	AK25
M. B, DQ#104	AK25
M. B, DQ#105	AK25
M. B, DQ#106	AK25
M. B, DQ#107	AK25
M. B, DQ#108	AK25
M. B, DQ#109	AK25
M. B, DQ#110	AK25
M. B, DQ#111	AK25
M. B, DQ#112	AK25
M. B, DQ#113	AK25
M. B, DQ#114	AK25
M. B, DQ#115	AK25
M. B, DQ#116	AK25
M. B, DQ#117	AK25
M. B, DQ#118	AK25
M. B, DQ#119	AK25
M. B, DQ#120	AK25
M. B, DQ#121	AK25
M. B, DQ#122	AK25
M. B, DQ#123	AK25
M. B, DQ#124	AK25
M. B, DQ#125	AK25
M	





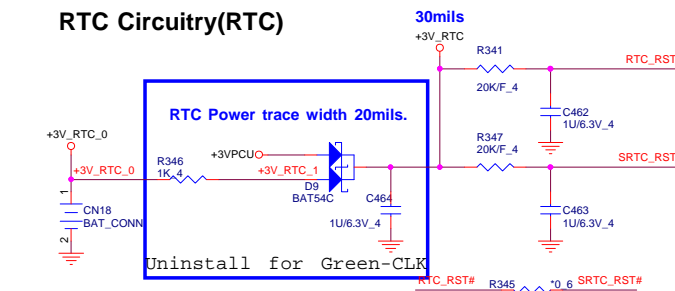


07

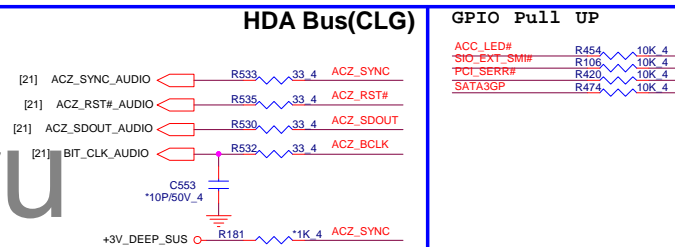


no stuff If use green Clock

RTC Circuitry(RTC)



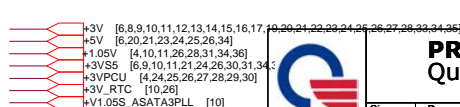
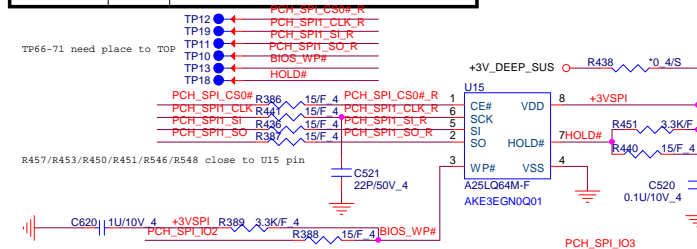
HDA Bus(CLG)



GPIO Pull UP

☐ PCH SPI ROM(CLG)

Vender	Size	P/N
AMIC	8MB	AKE3EFN0800 (A25LQ64M-F)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023



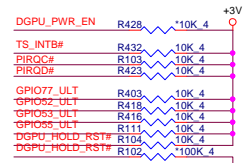
PROJECT :JWU
Quanta Computer Inc.

Size Custom	Document Number ULT 6/9(SATA/HDA)	Re 3
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PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up							
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overriden							
GPIO0_MOSI /GPIO86	Boot BIOS Selection	PWROK	<table border="1"><thead><tr><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>LPC</td></tr><tr><td>0</td><td>SPI(Default)</td></tr></tbody></table>	GNT0#	Boot Location	1	LPC	0	SPI(Default)	
GNT0#	Boot Location									
1	LPC									
0	SPI(Default)									
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality							
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up							

PCI/USB OC# Pull-up (CLG)

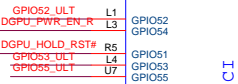
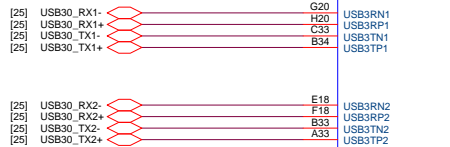


+3V_DEEP_SUS
📍 for DS3

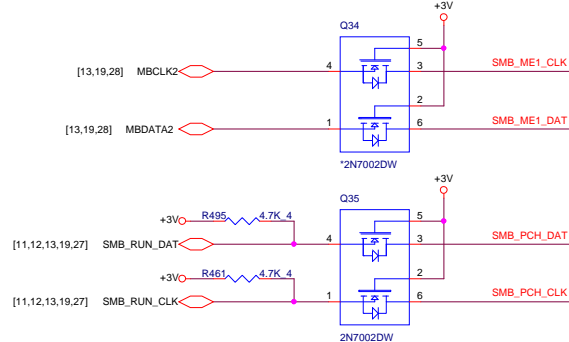


USB3.0

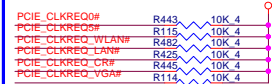
20111130 Modify USB3.0 for HM70



SMBus/Pull-up(CLG)

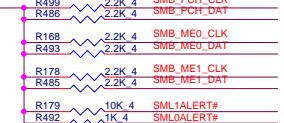


CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)

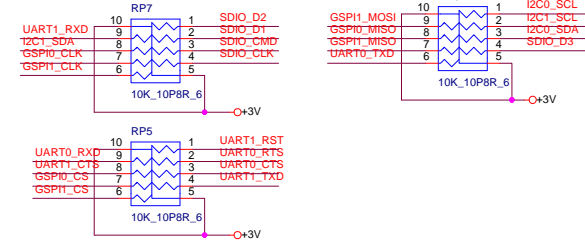
for DS3



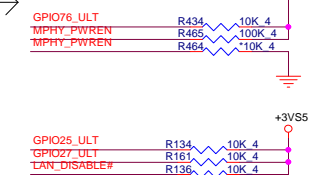
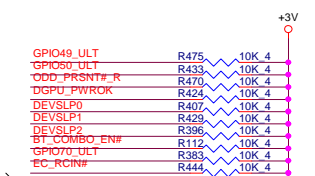
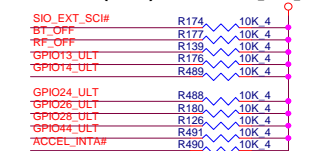
PROJECT :JWU
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+3V_DEEP_SU



*V1 05S VCCS

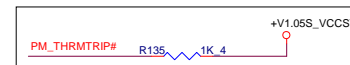


Diagram illustrating a 5x2 grid of resistors (R132, R158, R155, R160, R463, R128 in the left column; R133, R159, R154, R167, R466, R127 in the right column) connected to a 3V_DEEP_SUS supply. The resistors are labeled with their reference designators, values (*10K 4), and board IDs (BOARD_ID0 to BOARD_ID5). The diagram also includes a table mapping the board IDs to the corresponding Ra and Rb values.

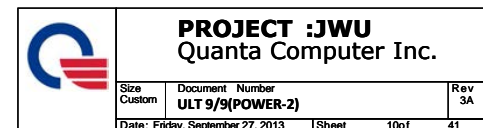
	DIS
Stuff	Ra
NC	Rb

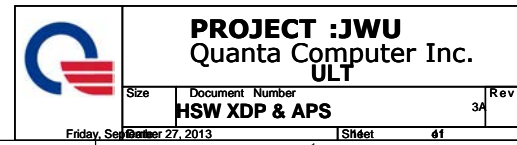
	DIS	UMA
Stuff	Ra	Rb
NC	Rb	Ra

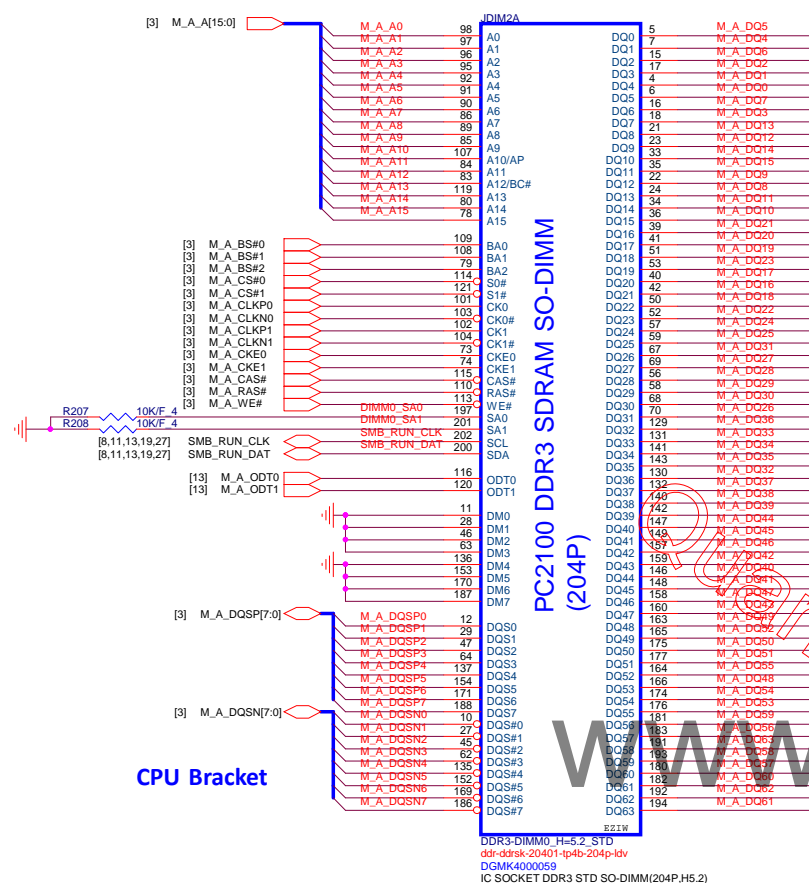


PROJECT :JWU
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Size Custom	Document Number ULT 8/9 (GPIO/MISC)	Rev 3A
Date: Friday, September 27, 2013	Sheet	9 of 41

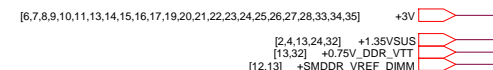
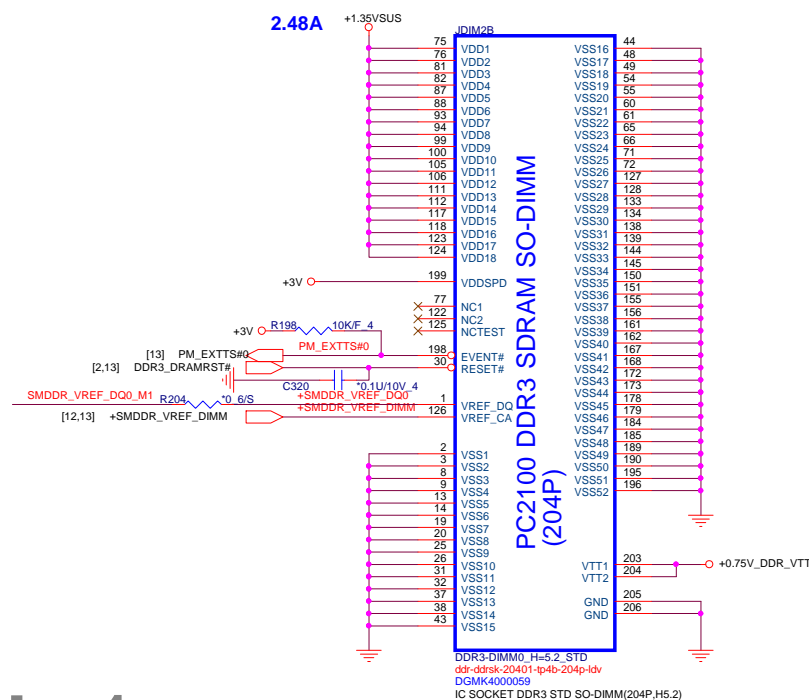




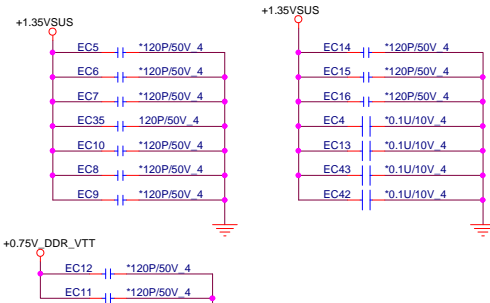


CPU Bracket

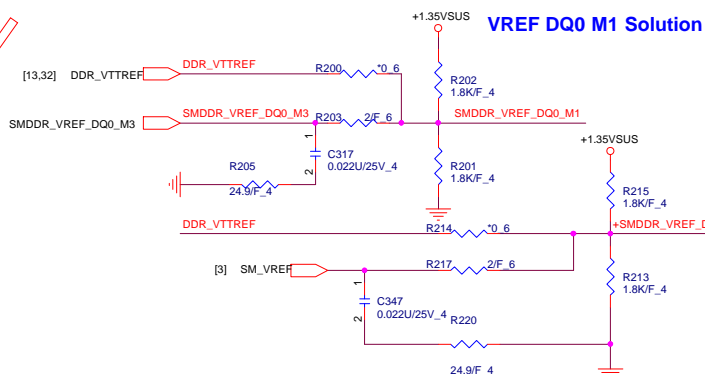
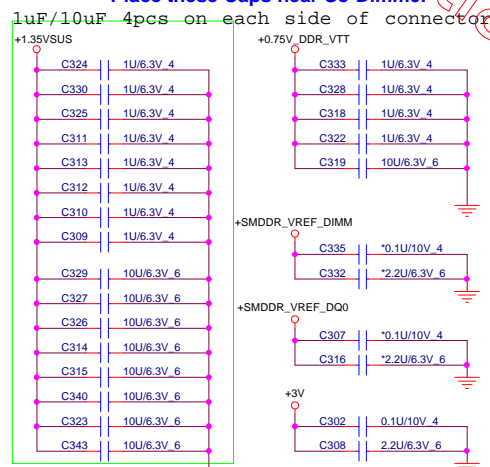
M_A_DQ[63:0] [3]

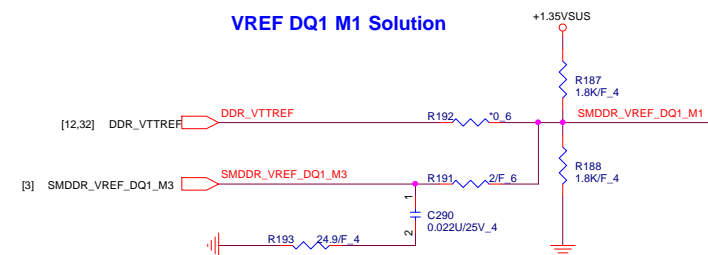
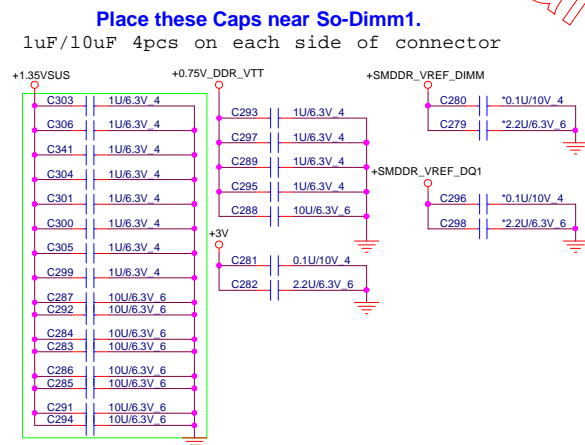
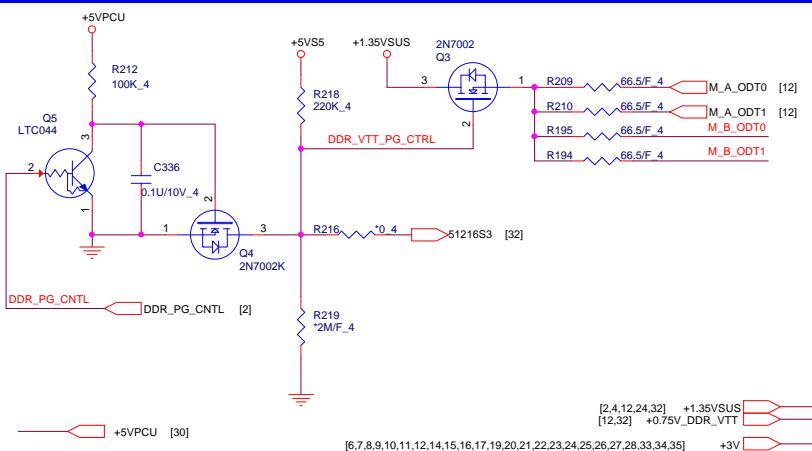
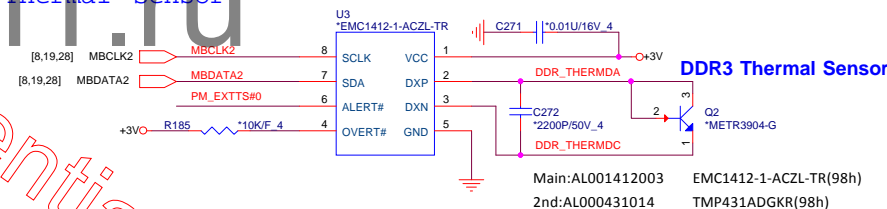
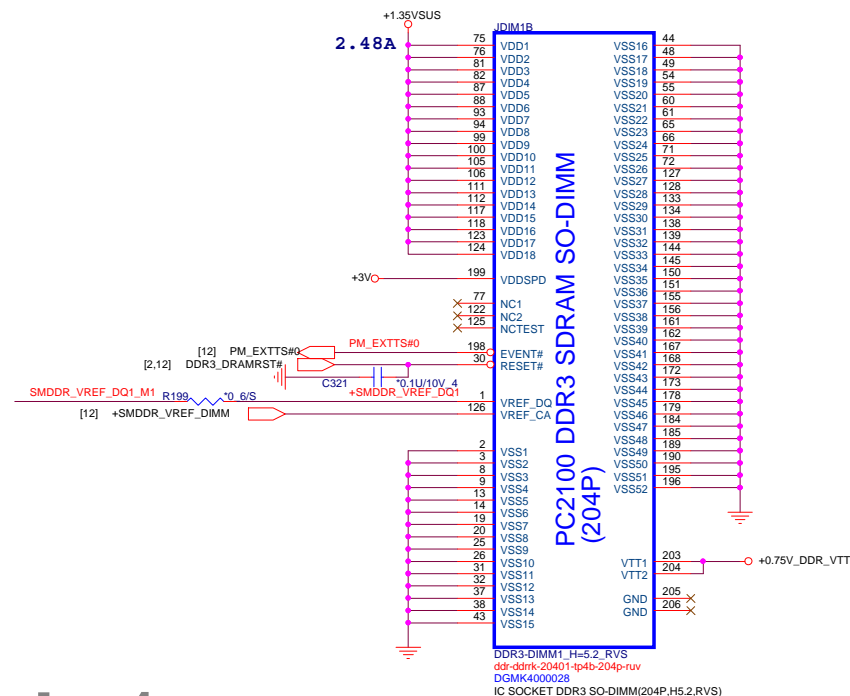


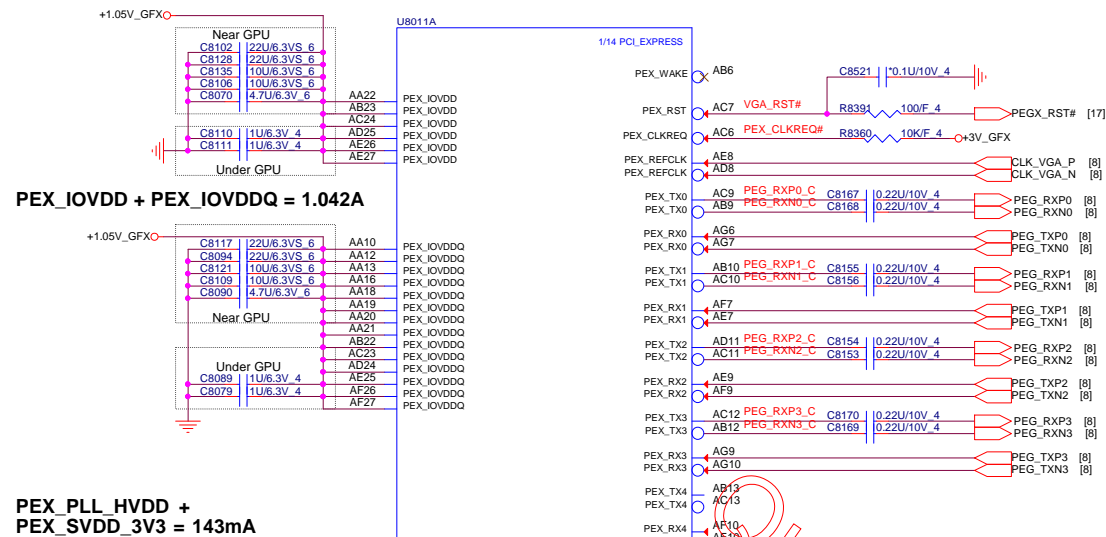
For EMI RESERVE

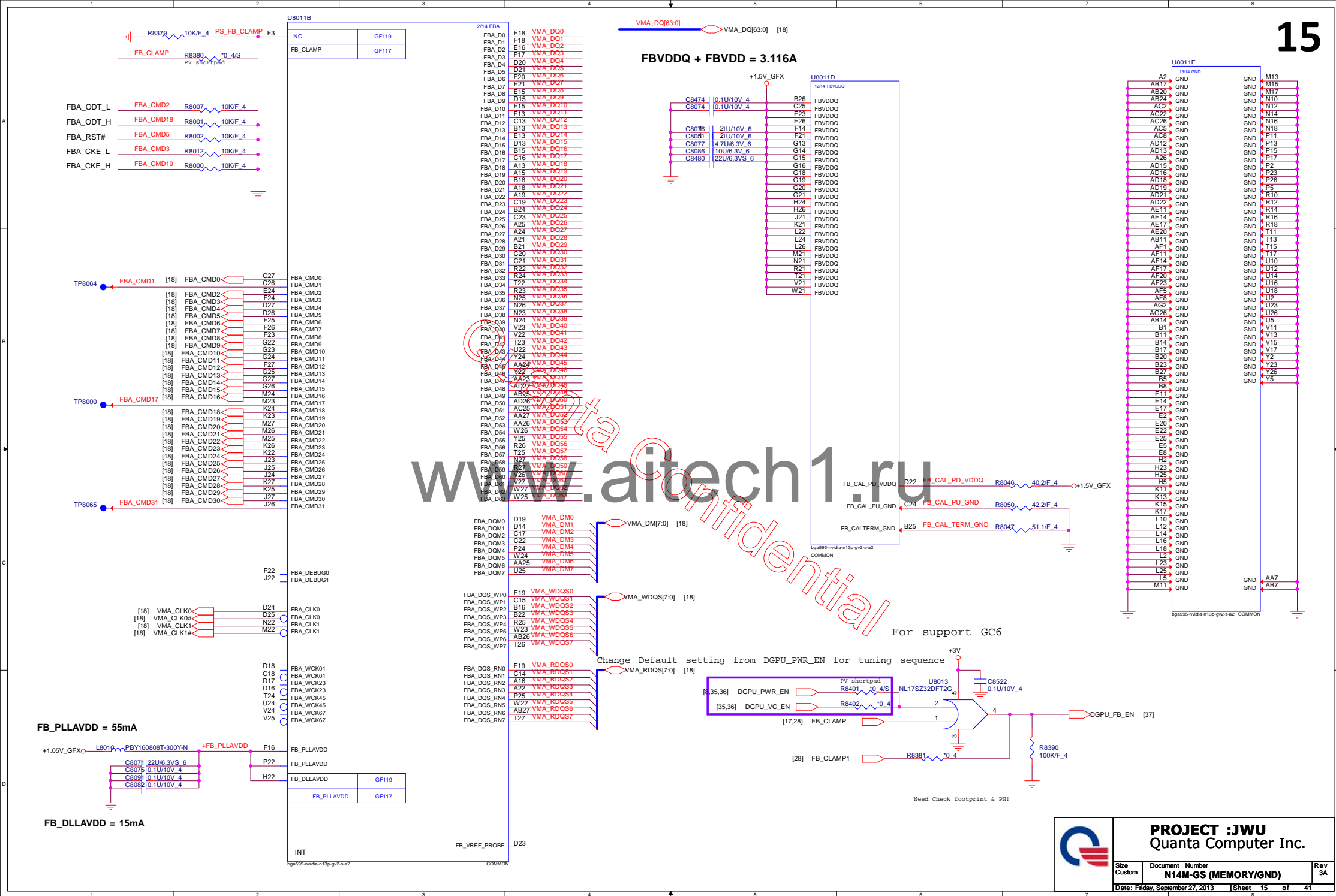


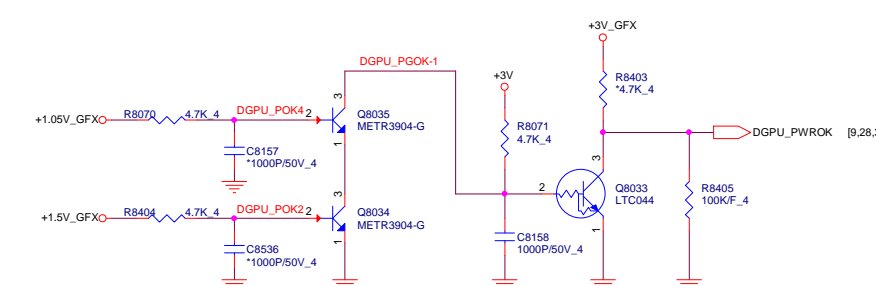
Place these Caps near So-Dimm0.













VRAM (DDR3 / 900MHz) Configuration Table ROM_SI	
2G Samsung 256Mx16x4	20K PD
2G Micron 256Mx16x4	10K PD
2G Hynix 256Mx16x4	15K PD

Netname	N14P-GV2
ROM_SO	5K PU
ROM_SCLK	5K PU
STRAP0	45K PU
STRAP1	45K PD
STRAP2	15K PD
STRAP3	5K PD
STRAP4	45K PD

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

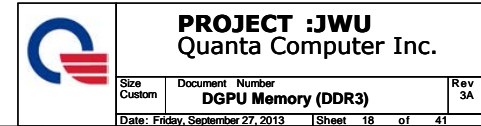
DDR3 Type		Configuration	Size
Samsung K4W4G1646B-HC11 Quanta P/N: AKD5MGWT516	(4G bits)	256 * 16 x 4 pcs	2G
Micron MT41K256M16HA-107G-E Quanta P/N: AKD5PGSTL00	(4G bits)	256 * 16 x 4 pcs	2G
Hynix H5TC4G63AFR-11C Quanta P/N: AKD5PGWTW05	(4G bits)	256 * 16 x 4 pcs	2G



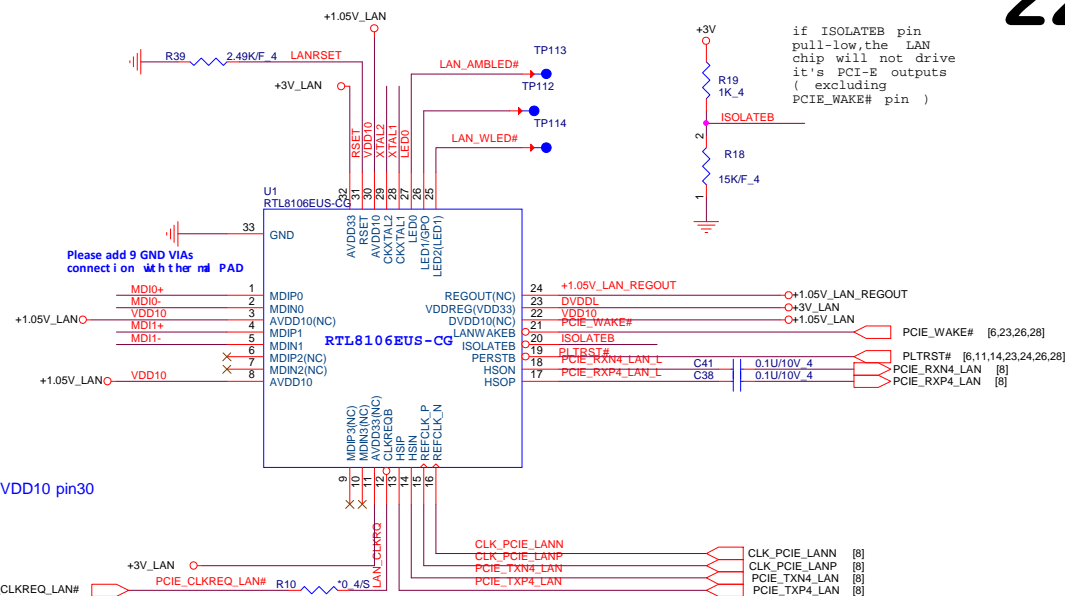
PROJECT :JWU
Quanta Computer Inc.

Size Custom	Document Number N14M-GS (GPIO/STRAPS)	Rev 3A
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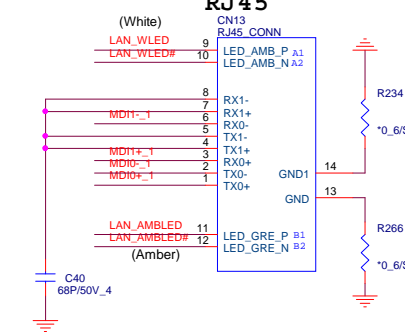




```
if ISOLATEB pin
pull-low,the LAN
chip will not drive
it's PCI-E outputs
( excluding
PCIE WAKE# pin )
```

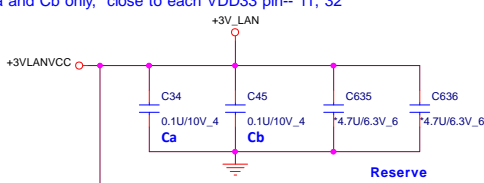
TWD Type

RJ45



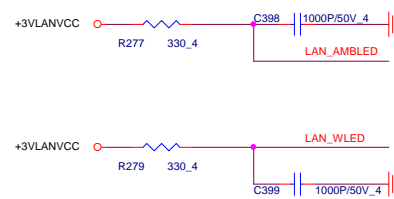
BOT: TST1284R LF DB0EL5LAN00


Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



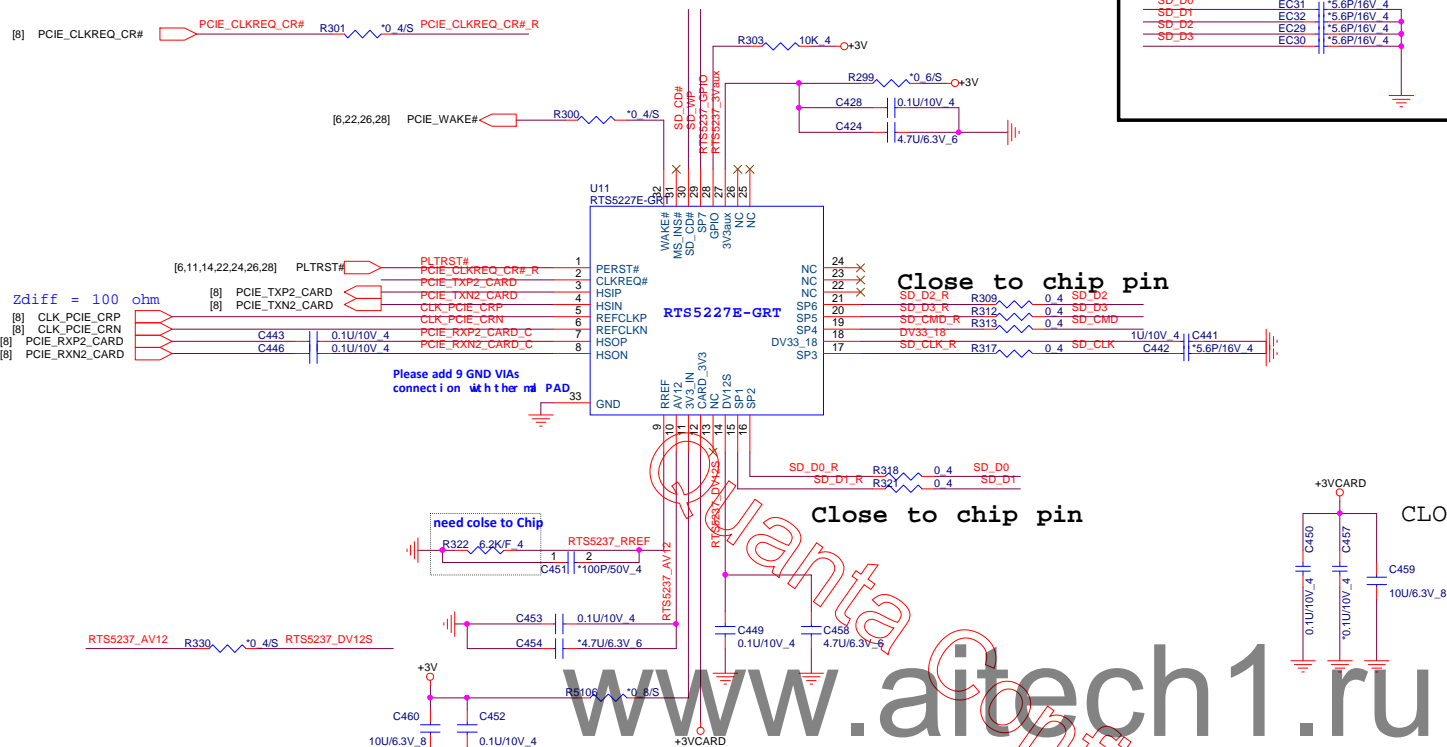
Place Cc and Cd close to each VDD33 pin-- 11, 32

Remove For Not Using SWR mode



	PROJECT :JWU Quanta Computer Inc.		
	Size Custom	Document Number LAN RTL8106E-CG/RJ45	Rev 3A
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Reserve for EMI

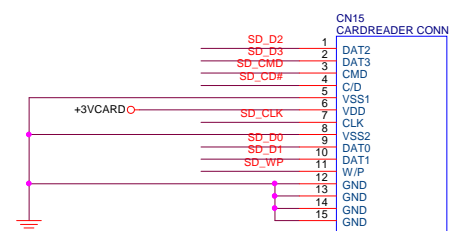


SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS

Share Pin

SD / MMC

CARD READER

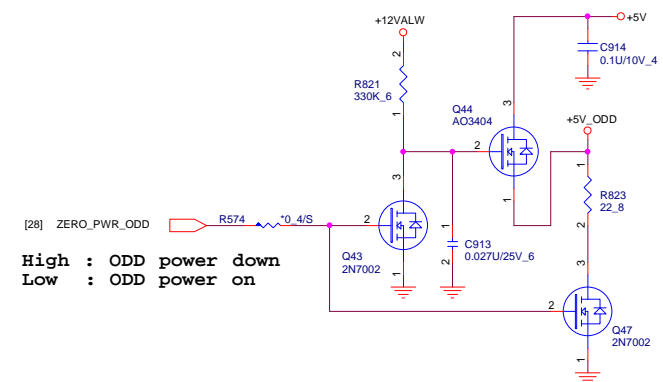
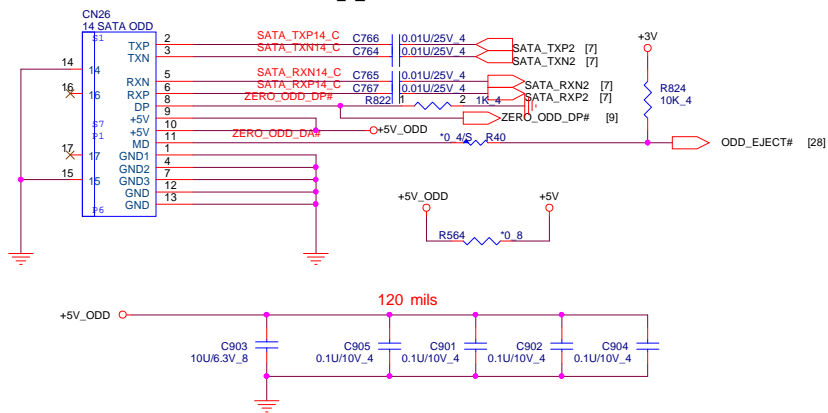


R3X Type

**SATA ODD
CONNECTOR**

14" SATA ODD

Bypass CAP close conn



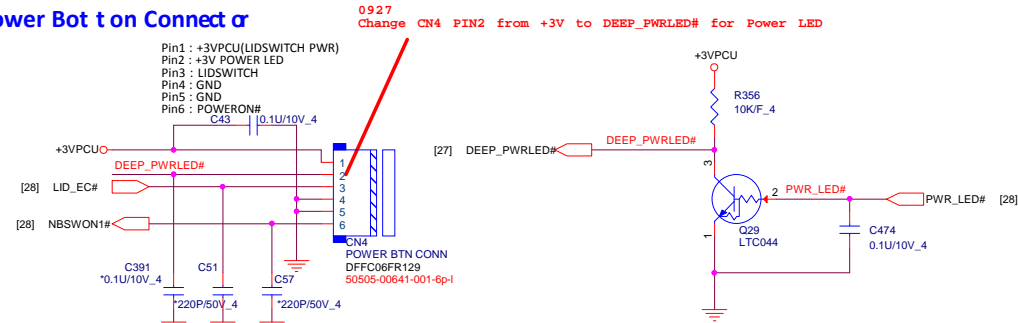
High : ODD power down
Low : ODD power on



PROJECT :JWU
Quanta Computer Inc.

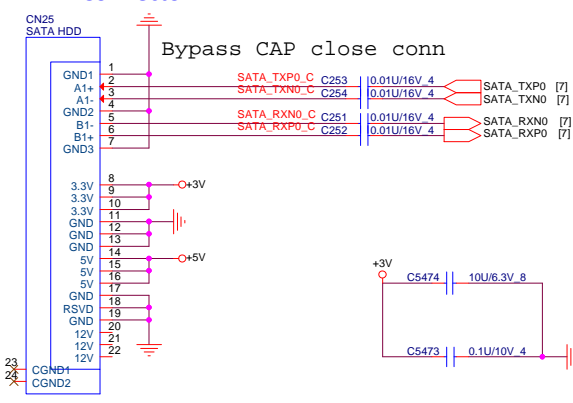
Size Custom	Document Number RTS5227E-GRT&CR SOCKET	Rev 3A
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Power Button Connector

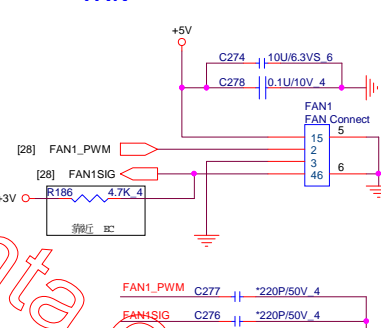


0327 :
DEL Touch Pad Connector CN7 for U83

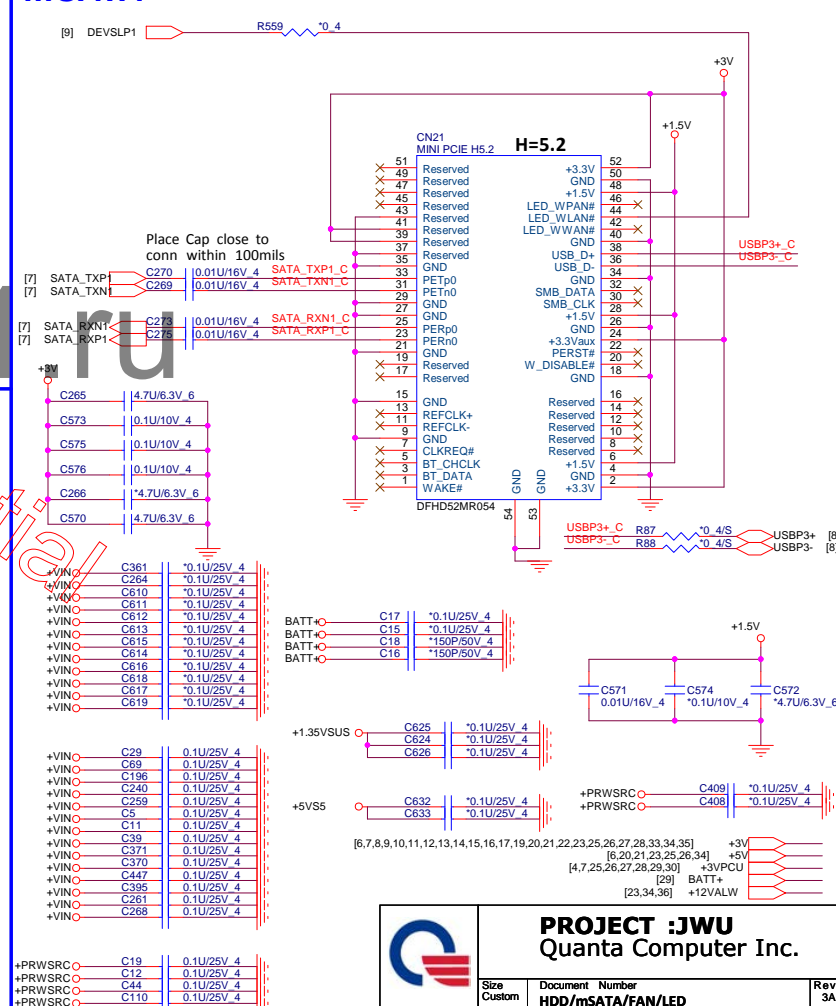
SATA HDD Connector



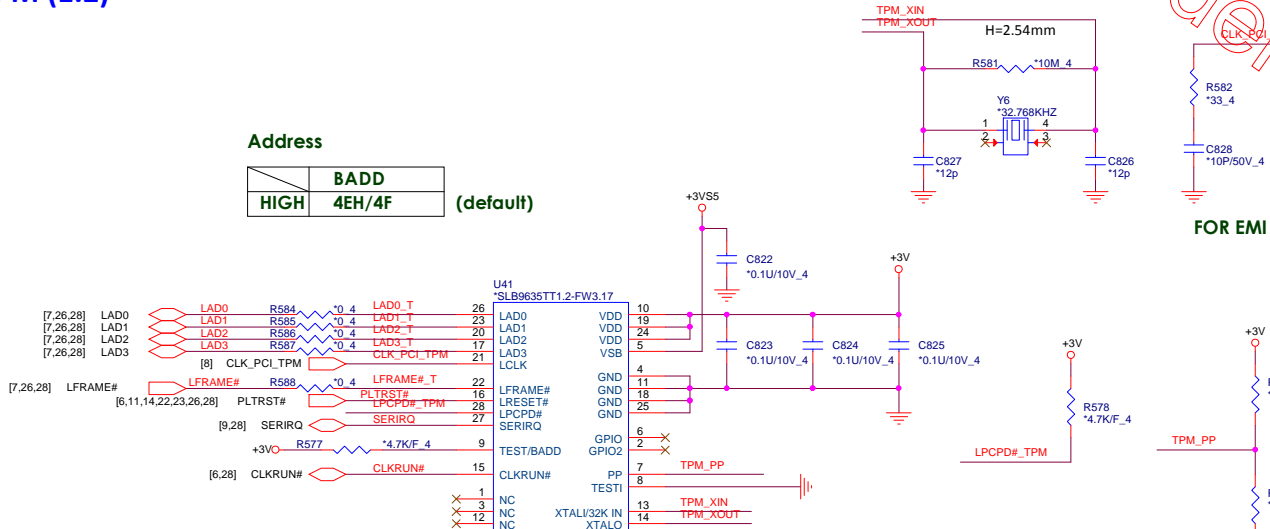
FAN



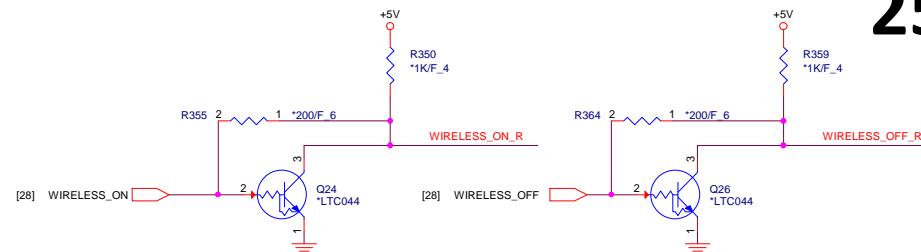
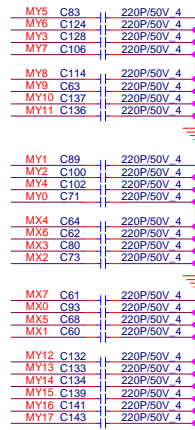
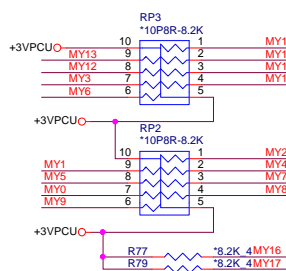
Mini PCI-E Card 2- Full size mSATA



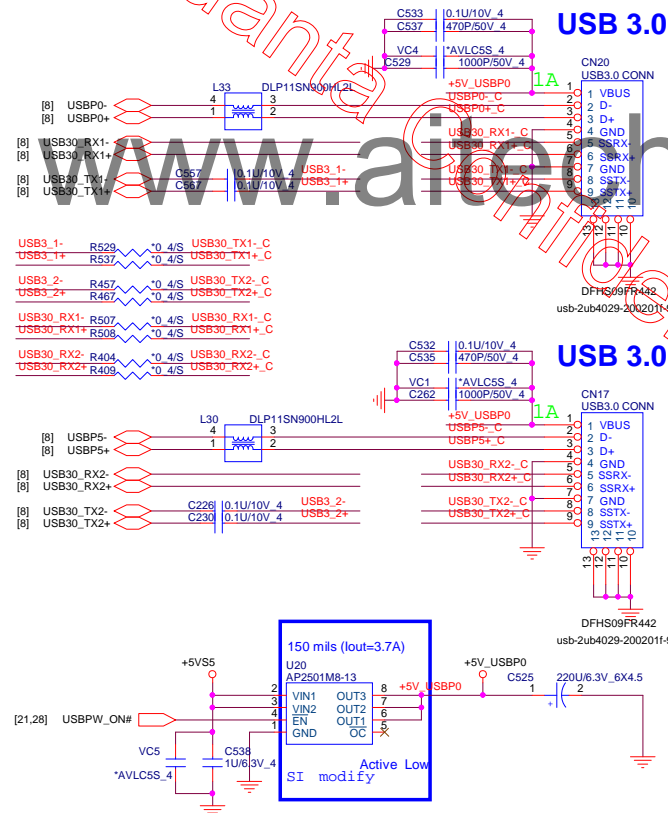
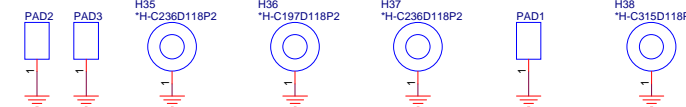
TPM (1.2)



The schematic diagram illustrates the MUTE_LED_CNTL_R1 circuit. It features a MOSFET Q21 (2N7002K) configured as a switch. The gate of Q21 is connected to the MUTE_LED_CNTL signal (pin [21]) through a 10K resistor R348. The drain of Q21 is connected to the MY[0..17] and MX[0..7] signal lines (pin [28]). The source of Q21 is connected to ground.



0402 :
ADD H38 HOLE



H30
*INTEL-BKT-SHARK-ULT

H33
*H-TC279BC216D141P2

H34
*H-TC279BC216D141P2

H17
*H-C394D118P2

H13
*H-C394D118P2

H20
*H-C394D118P2

H10
*H-TC279BC216D141P2

H19
*H-C315D118P2

H24
*H-C393D354P2

H18
*H-C394D118P2

H15
*H-C394D118P2

H25
*H-C315D102P2

H27
*H-TC236BC315D145P2

H28
*H-C236D104P2

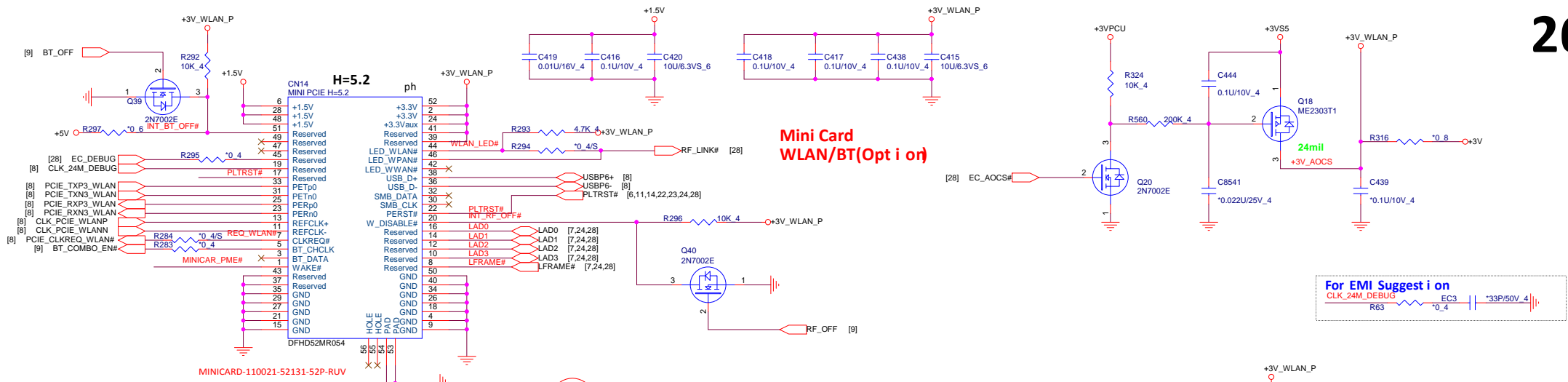
H29
*H-TC236BC287d145P

H22
*O-U6X-2

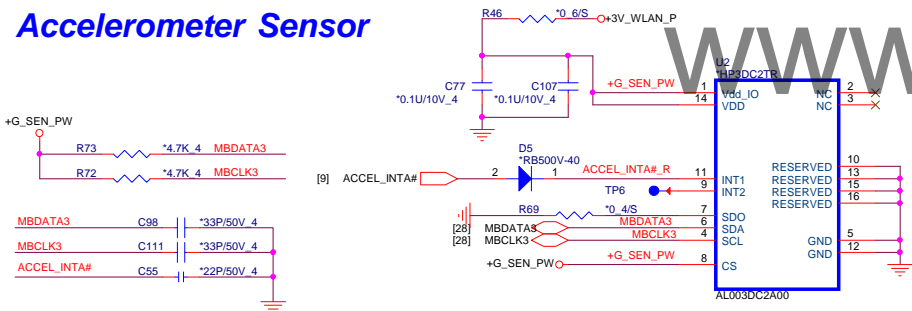
Mini-PCIe & mSATA nut
Nut PN:MBZR7001010



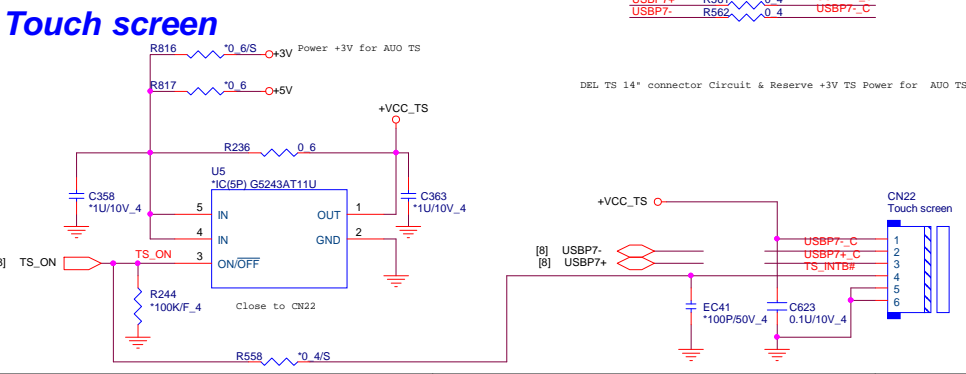
Size Custom	Document Number USB3.0/KB	Rev 3A
Date: Friday, September 27, 2013		Sheet 25 of 41



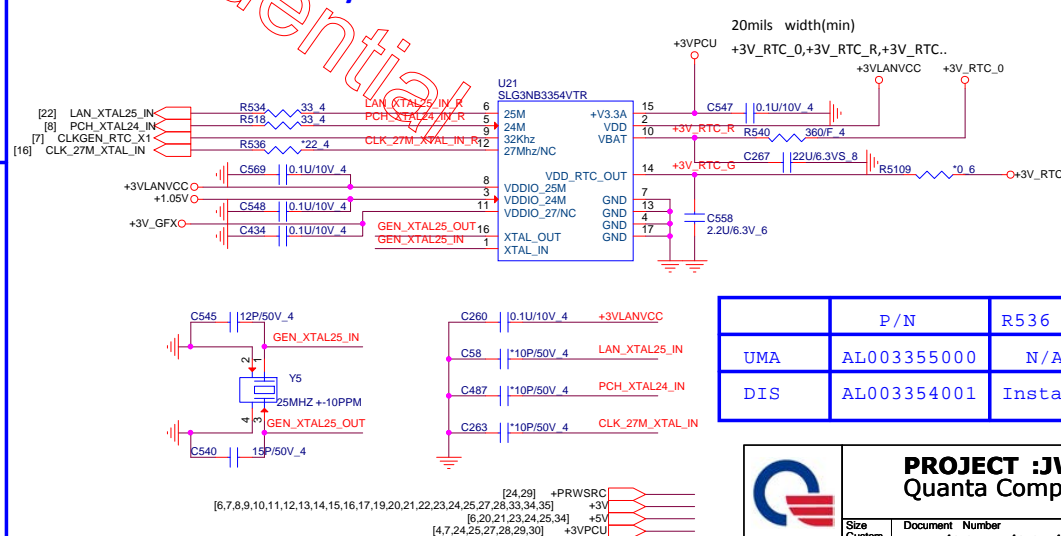
Accelerometer Sensor



Touch screen



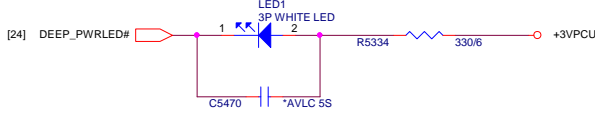
Green CLK Circuitry



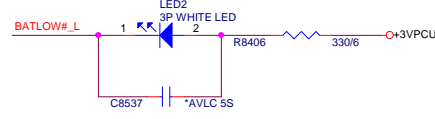
	P/N	R536	C434
UMA	AL003355000	N/A	N/A
DIS	AL003354001	Install	Instal

LED Status

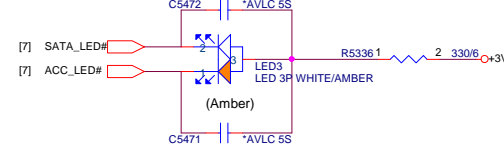
PWR LED



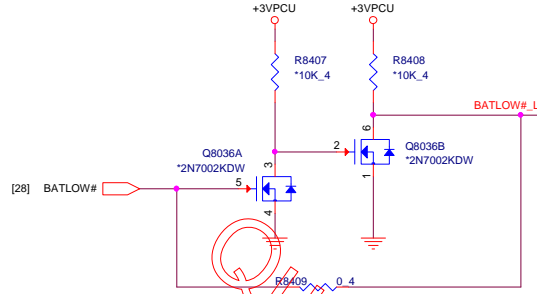
BAT LED



SATA LED



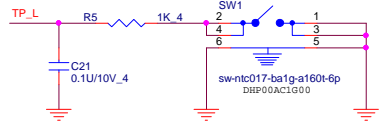
2013/07/05 Reserve for BATTERY LED



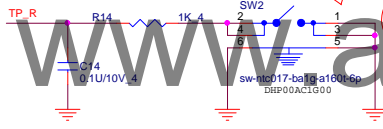
Function Button

0327 :
ADD SW1/SW2/R14/R5/C14/C21 Function on Button for JWU

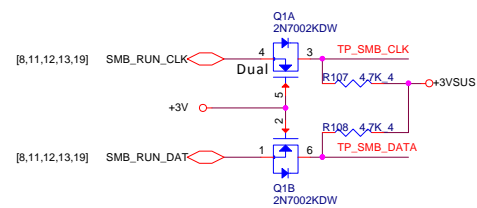
Left



Right

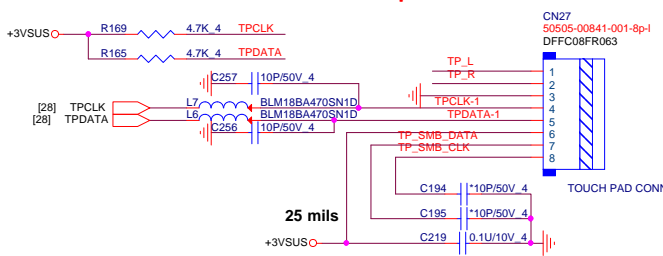


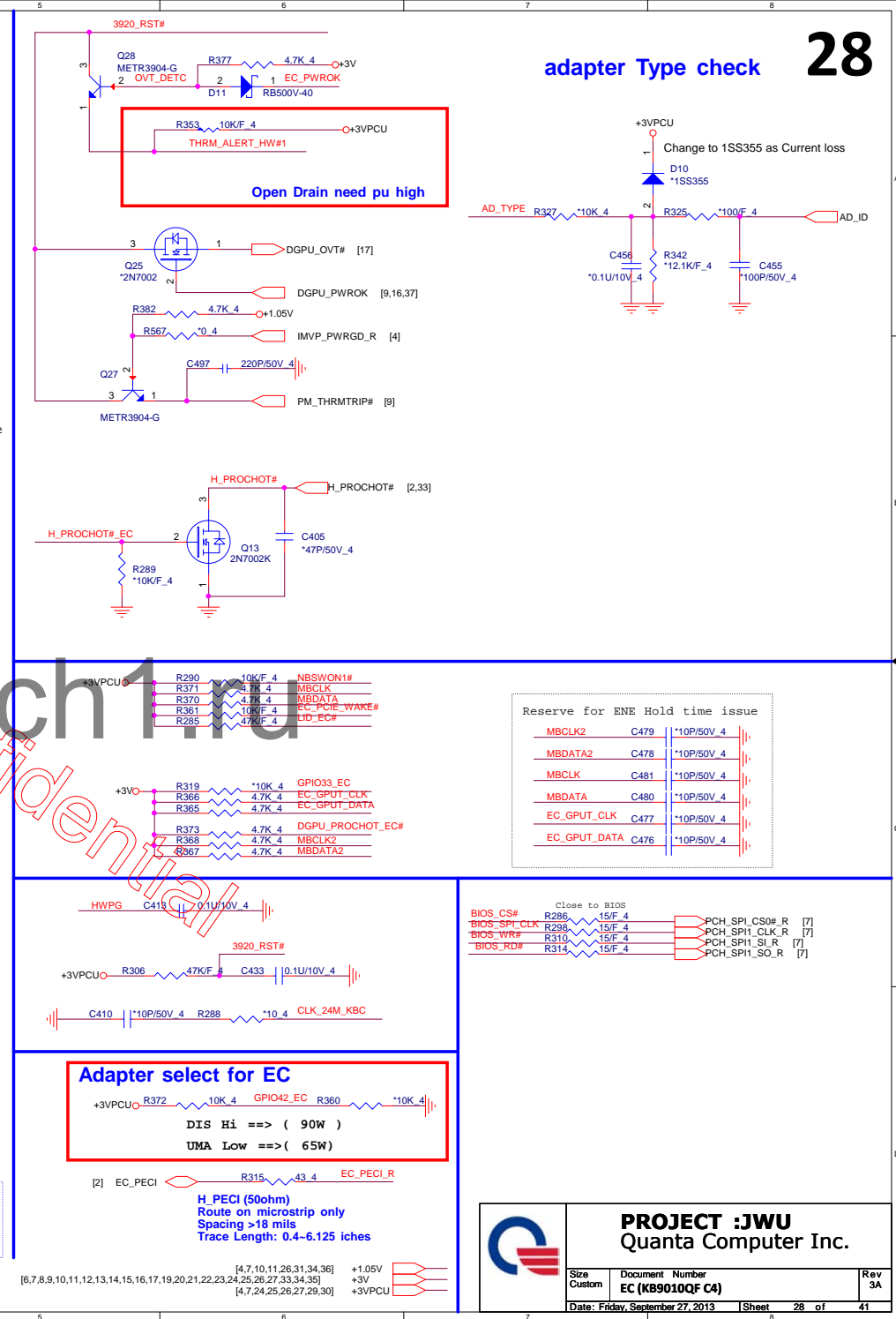
Touch Pad Connector

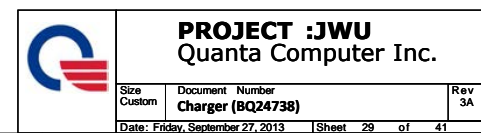


To Touch pad

0327 :
ADD Touch Pad Connector CN27 for JWU

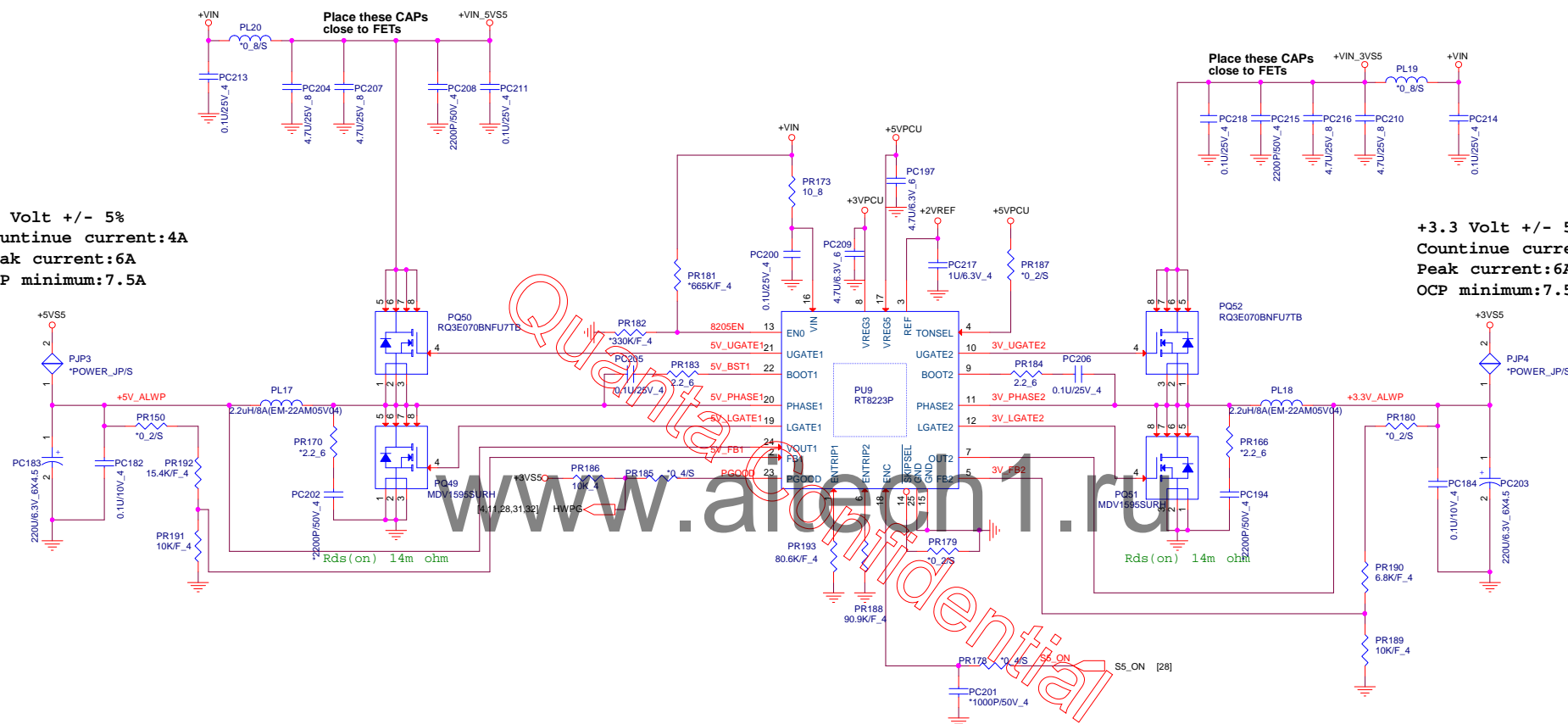


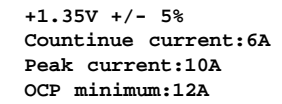


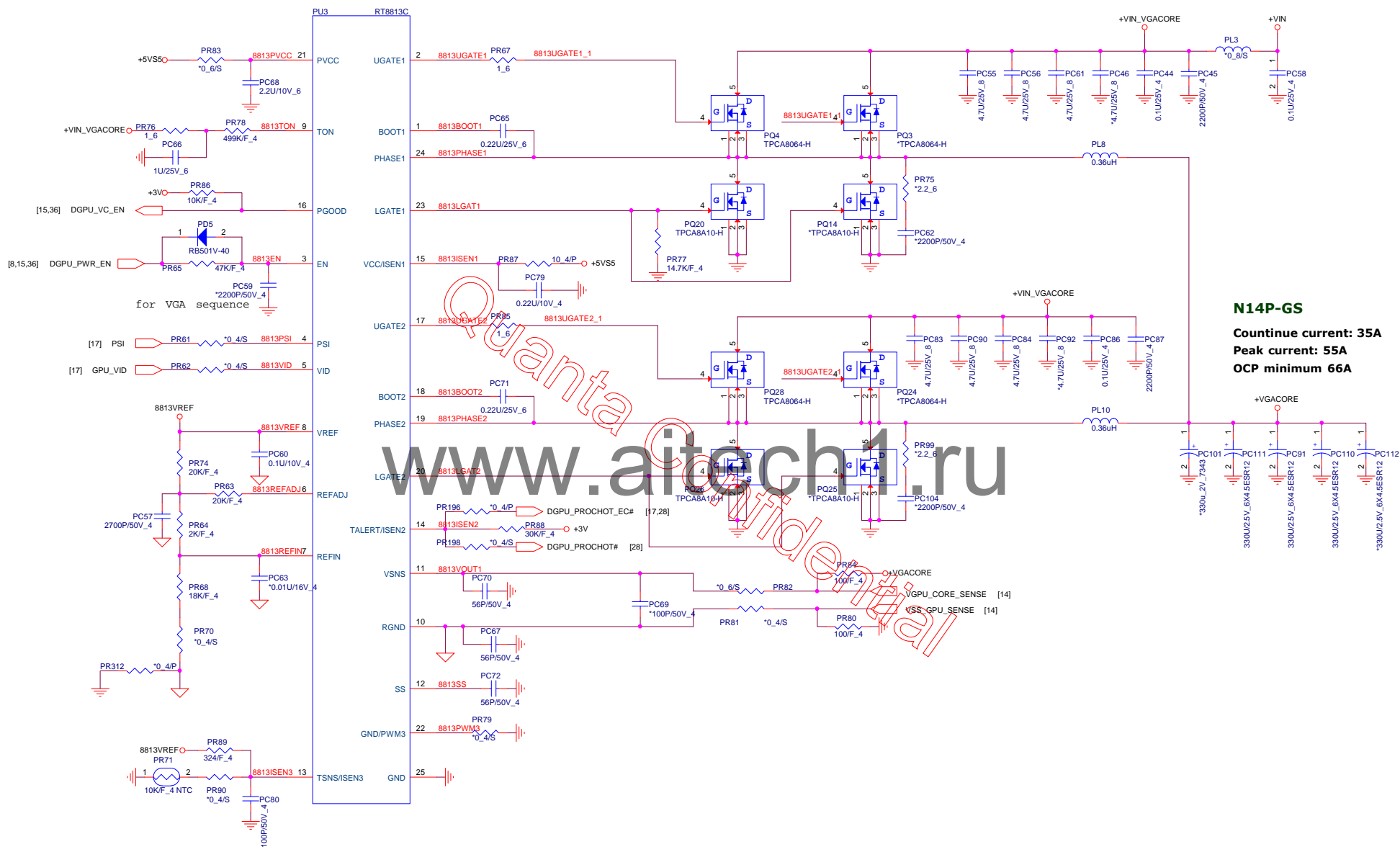


+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

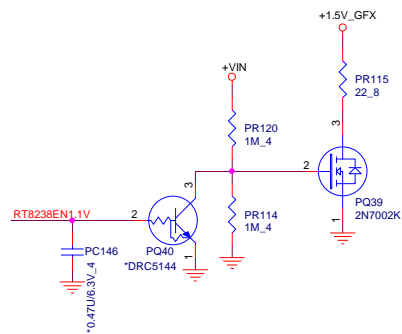
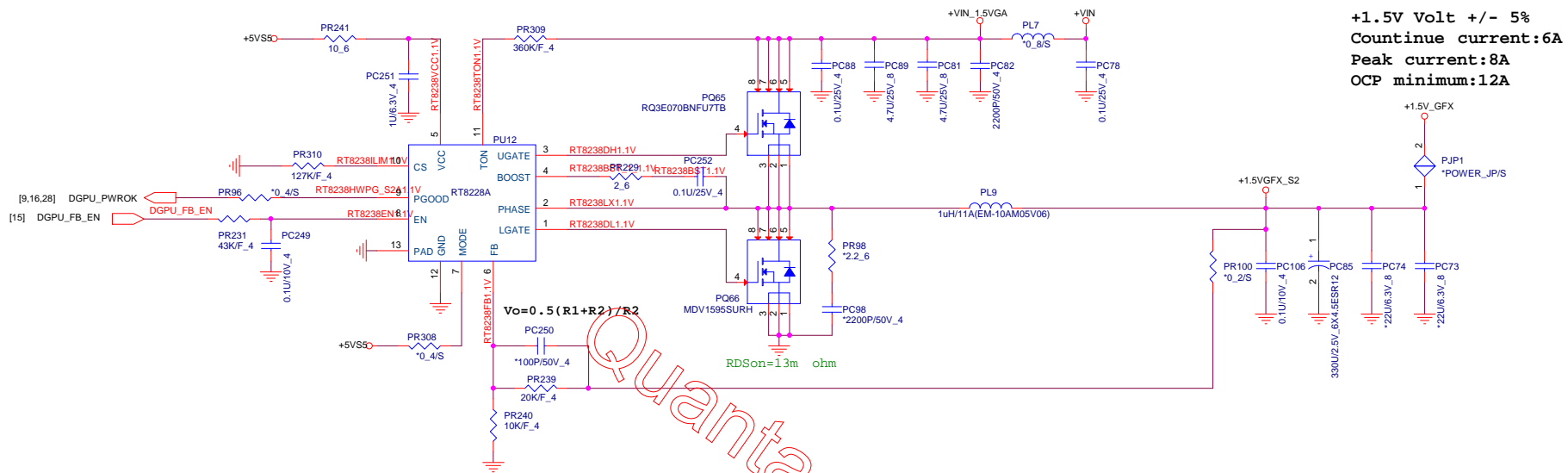
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A







N14P-GS
Countinue current: 35A
Peak current: 55A
OCP minimum 66A



USB3.0	Port Assignment	Power control pin
PORT1	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT3	NC	N/A
PORT4	NC	N/A

USB2.0	Port Assignment	Power control pin
PORT0	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT1	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT2	Camera	N/A
PORT3	NC	N/A
PORT4	NC	N/A
PORT5	Left side USB daughter B	USBPW_ON#(from EC)
PORT6	WLAN	N/A
PORT7	Touch Screen 15" used	TS_ON(from EC)

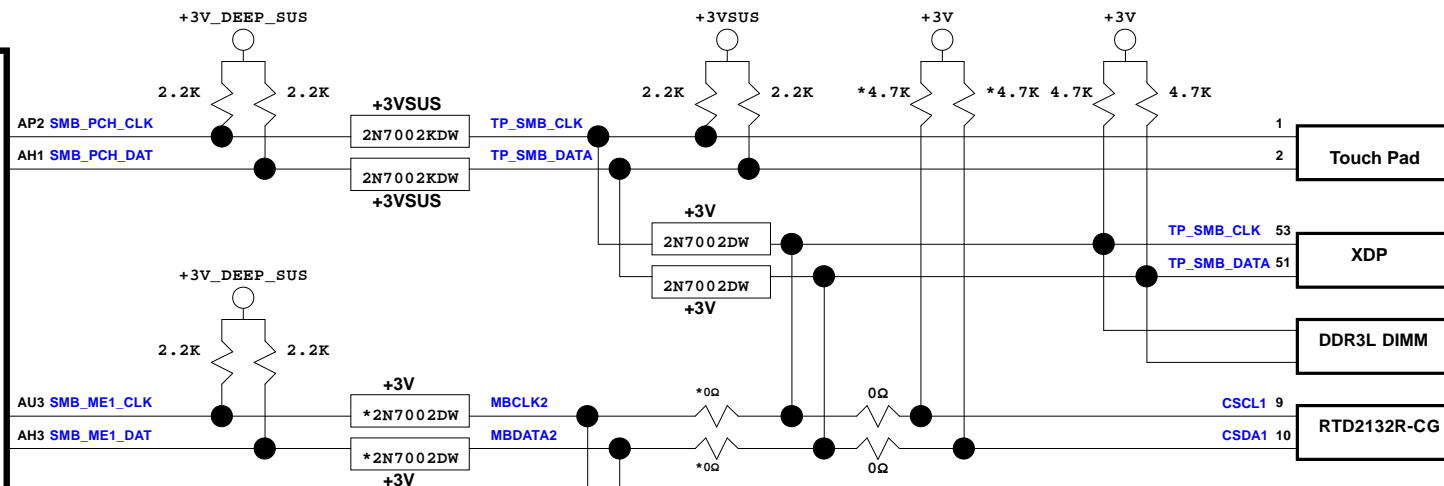
SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	mSATA	N/A
SATA2	NC	N/A
SATA3/PCIE	Card reader	N/A

PCIE	Port Assignment	Control pin
PCIE 5_L0	PEG0	
PCIE 5_L1	PEG1	
PCIE 5_L2	PEG2	
PCIE 5_L3	PEG3	
PCIE 1	NC	
PCIE 2	NC	
PCIE 3	WLAN	
PCIE 4	LAN	

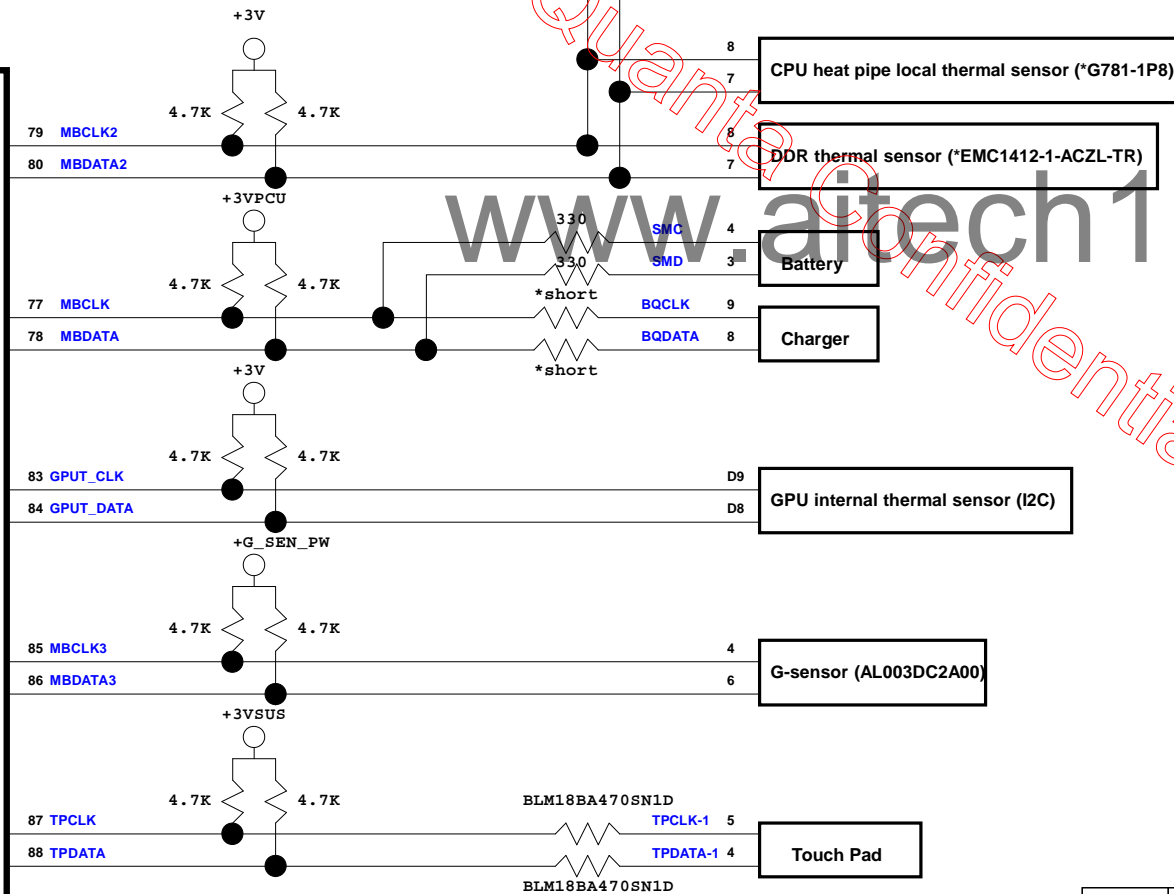


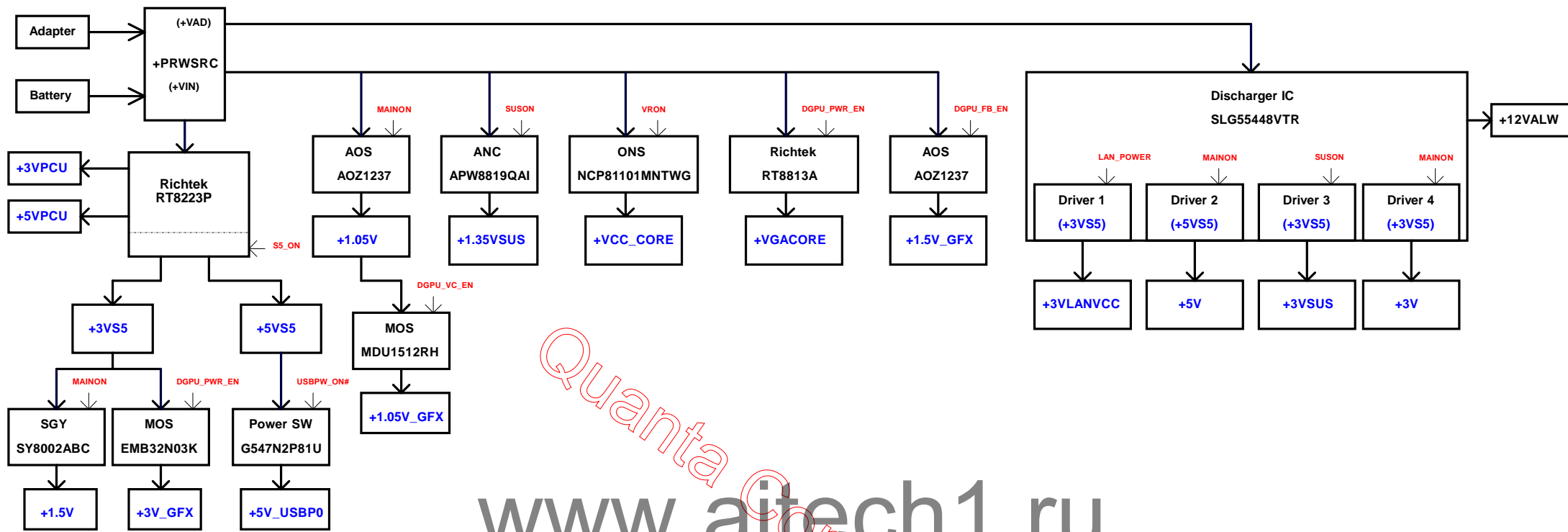
PROJECT :JWU
Quanta Computer Inc.

Haswell
ULT

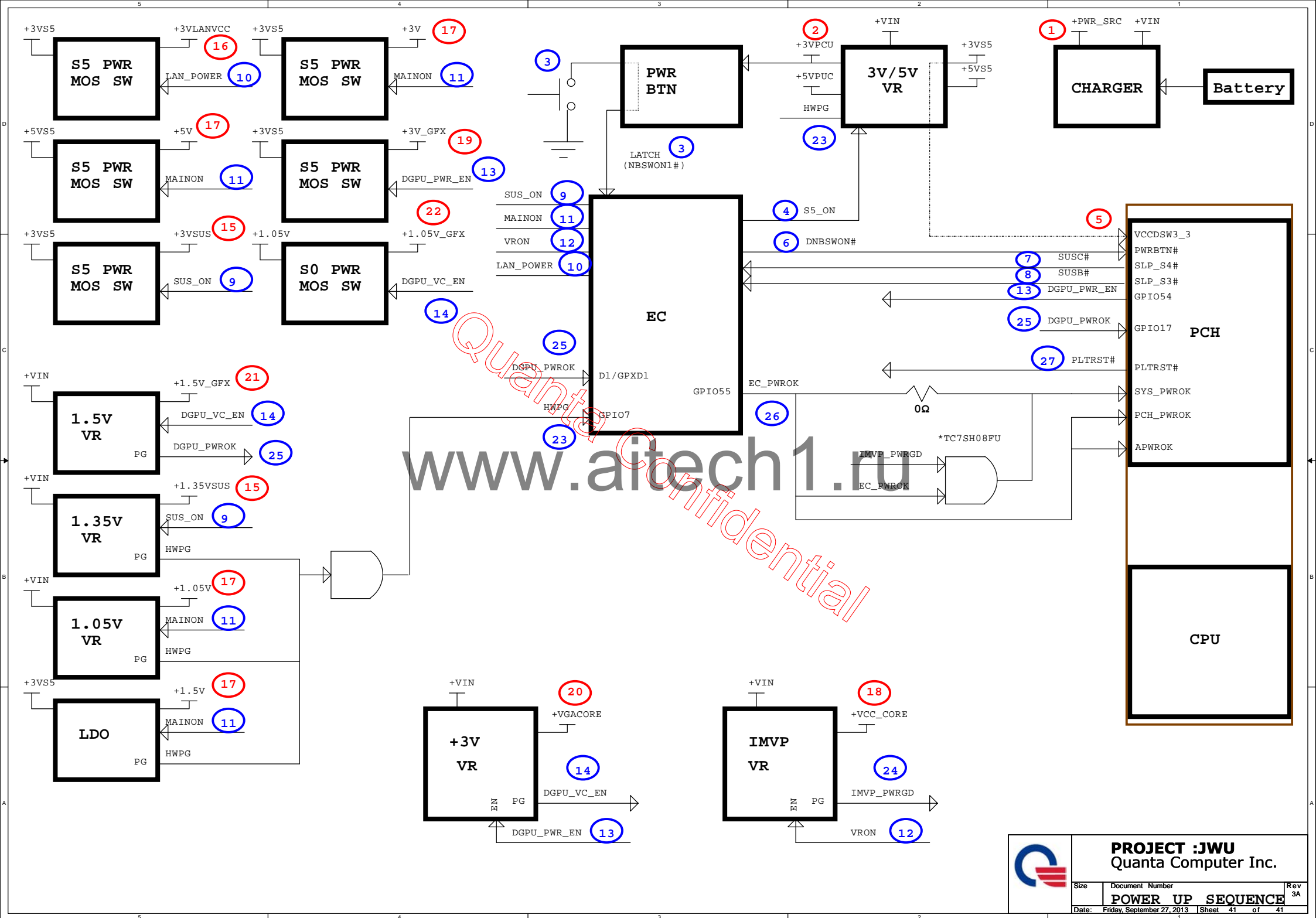


EC
KB9010QF





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PROJECT :JWU
Quanta Computer Inc.

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